ABSTRACT OF THE INVENTION

With respect to each application, libraries, corresponding to operation models, for describing operations respectively attained by employing a Neumann CPU (bus structure), a Harvard CPU (bus structure) and a direction separate type CPU (bus structure) are registered. In a performance table of each library, the performance index of the library is expressed as a function of parameters of throughput, a bus width, instruction quantity and memory size. Also, a portion of the operation realized by using software and a portion realized by using hardware are registered. Through operation simulation conducted with each application successively replaced with each of the libraries, the performance of a semiconductor integrated circuit can be evaluated, so as to synthesize an optimal interface.